



KM1248 Hall-effect sensor is a temperature stable, stress-resistant , micro-power switch. Superior high-temperature performance is made possible through a dynamic offset cancellation that utilizes chopper-stabilization. This method reduces the offset voltage normally caused by device over molding, temperature dependencies, and thermal stress.

KM1248 includes the following on a single silicon chip: voltage regulator, Hall voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, open-drain output. Advanced CMOS wafer fabrication processing is used to take advantage of low-voltage requirements, component matching, very low input-offset errors, and small component geometries.

This device requires the presence of omni-polar magnetic fields for operation.

KM1248 is rated for operation between the ambient temperatures -40°C and $+85^{\circ}\text{C}$ for the E temperature range. The four package styles available provide magnetically optimized solutions for most applications. Package types SO is an SOT-23(1.1 mm nominal height), SQ is an QFN2020-3(0.5 mm nominal height), Tsot-23 is an ST(0.7 mm nominal height) ,a miniature low-profile surface-mount package, while package UA is a three-lead ultra-mini SIP for through-hole mounting.

The package type is in a lead Halogen Free version was verified by third party Lab.

Features and Benefits

- CMOS Hall IC Technology
- Solid-State Reliability
- Micro power consumption for battery-powered applications
- Omni polar, output switches with absolute value of North or South pole from magnet
- Operation down to 1.8 V and Max at 5.5V.
- High Sensitivity for direct reed switch replacement applications
- Multi Small Size option
- Custom sensitivity selection is available in optional package.
- Pb Free/Green chip is qualified by third party lab.

Applications

- Solid state switch
- Handheld Wireless Handset Awake Switch (Flip Cell/PHS Phone/Note Book/Flip Video Set)
- Lid close sensor for battery powered devices
- Magnet proximity sensor for reed switch replacement in low duty cycle applications

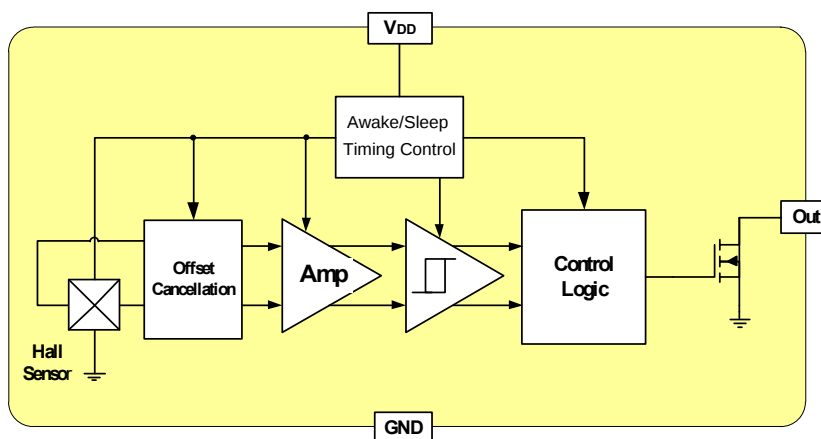


Ordering Information

XX XX XX X - X Company Name and Product Category Part number Temperature Code Package type Sorting Code	Company Name and Product Category Part number 181,D182,183,184,185,248,477,D381,D381F,381R,D382..... If part # is just 3 digits, the forth digit will be omitted. Temperature range E: 85 °C, I: 105 °C, K: 125 °C, L: 150 °C Package type UA:TO-92S,VK:TO-92S(4pin),VF:TO-92S(5pin),SO:SOT-23, SQ:QFN-3,ST:TSOT-23,SN:SOT-553,SF:SOT-89(5pin), SS:TSOT-26,SD:DFN-6,SG:SOT-89(3pin) Sorting α,β,Blank.....
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Part No.	Temperature Suffix	Package Type
KM1248EUA	E (-40°C to + 85°C)	UA (TO-92S)
KM1248ESO	E (-40°C to + 85°C)	SO (SOT-23)
KM1248EST	E (-40°C to + 85°C)	ST (TSOT-23)
KM1248ESQ	E (-40°C to + 85°C)	SQ (QFN2020-3)

Functional Diagram



Note: Static sensitive device; please observe ESD precautions. Reverse V_{DD} protection is not included. For reverse voltage protection, a 100Ω resistor in series with V_{DD} is recommended.



Absolute Maximum Ratings At ($T_a=25^{\circ}\text{C}$)

Characteristics		Values	Unit
Supply voltage,(VDD)		6	V
Output Voltage,(Vout)		6	V
Reverse voltage, (VDD) (VOUT)		-0.3	V
Magnetic flux density		Unlimited	Gauss
Output current(IOUT)		2	mA
Operating temperature range, (T_a)		-40 to +85	$^{\circ}\text{C}$
Storage temperature range, (T_s)		-55 to +150	$^{\circ}\text{C}$
Maximum Junction Temp,(T_j)		150	$^{\circ}\text{C}$
Thermal Resistance	(θ_{JA}) UA / SO / ST / SQ	206 / 543 / 310 / 543	$^{\circ}\text{C}/\text{W}$
	(θ_{JC}) UA / SO / ST / SQ	148 / 410 / 223 / 410	$^{\circ}\text{C}/\text{W}$
Package Power Dissipation, (PD) UA / SO / ST / SQ		606 / 230 / 400 / 230	mW

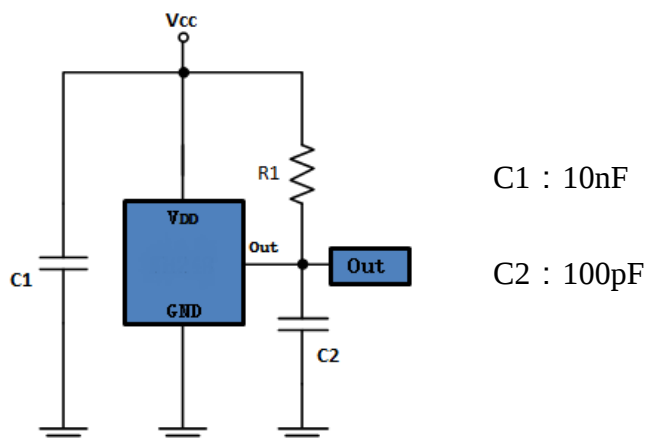
Note: Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Electrical Specifications

DC Operating Parameters $T_A=+25^{\circ}\text{C}$, $V_{DD}=3.0\text{V}$

Parameters	Test Conditions	Min	Typ	Max	Units
Supply Voltage,(VDD)	Operating	1.8		5.5	V
Supply Current,(IDD)	Awake State		2.5	4.0	mA
	Sleep State		8.0	12	μA
	Average		10	16	μA
Output Leakage Current,(Ioff)	Output off			1	μA
Output Low Voltage,(Vsat)	IOU=1mA			0.3	V
Awake mode time,(Taw)	Operating		70		μs
Sleep mode time,(TSL)	Operating		70		mS
Duty Cycle,(D,C)			0.1		%

Typical Application circuit



KM1248UA/SQ Magnetic Specifications

DC Operating Parameters $T_A = +25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.0\text{V}$

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operating Point	B _{OPS}	S pole to branded side, $B > BOP$, Vout On	6		60	Gauss
	B _{OPN}	N pole to branded side, $B > BOP$, Vout On	-60		-6	Gauss
Release Point	B _{RPS}	S pole to branded side, $B < BRP$, Vout Off	5		59	Gauss
	B _{RPN}	N pole to branded side, $B < BRP$, Vout Off	-60		-5	Gauss
Hysteresis	B _{HYS}	$ BOPx - BRPx $		7		Gauss

KM1248SO/ST Magnetic Specifications

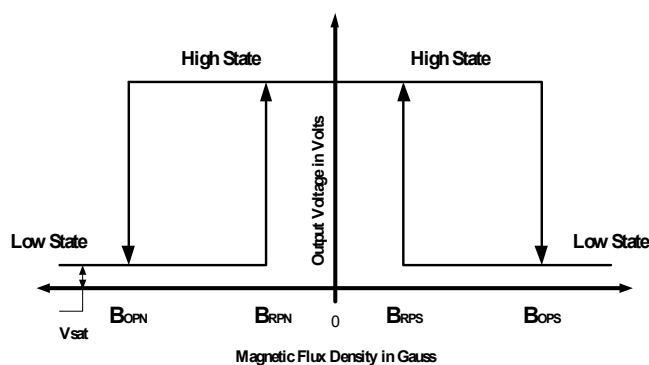
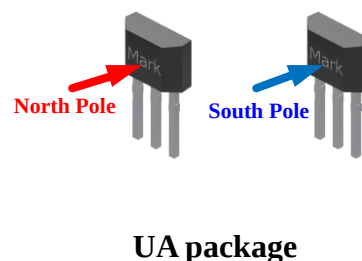
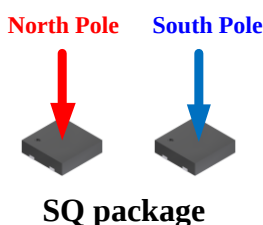
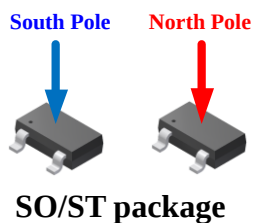
DC Operating Parameters $T_A = +25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.0\text{V}$

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operating Point	B _{OPS}	N pole to branded side, $B > BOP$, Vout On	6		60	Gauss
	B _{OPN}	S pole to branded side, $B > BOP$, Vout On	-60		-6	Gauss
Release Point	B _{RPS}	N pole to branded side, $B < BRP$, Vout Off	5		59	Gauss
	B _{RPN}	S pole to branded side, $B < BRP$, Vout Off	-60		-5	Gauss
Hysteresis	B _{HYS}	$ BOPx - BRPx $		7		Gauss

KM1248UA / SO / ST / SQ Output Behavior versus Magnetic Polar

DC Operating Parameters $T_a = -40\text{ to }85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.8\text{ V}$ and Max at 5.5V.

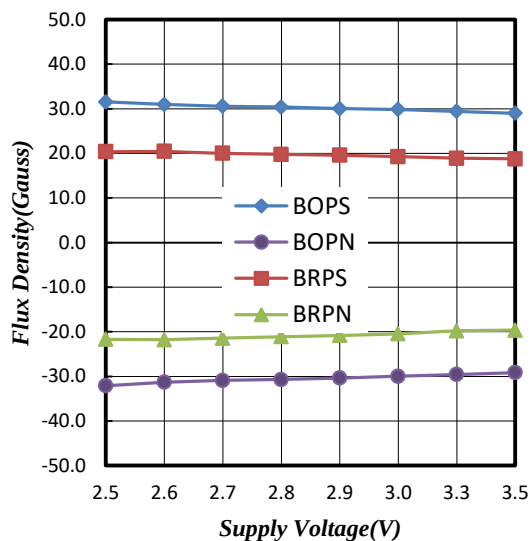
Parameter	Test condition	OUT(UA,SO,ST,SQ)
South pole	$B < Bop[(-60) \sim (-6)]$	Low
Null or weak magnetic field	$B = 0$ or $B < BRP$	Open(Pull-up Voltage)
North pole	$B > Bop(60 \sim 6)$	Low



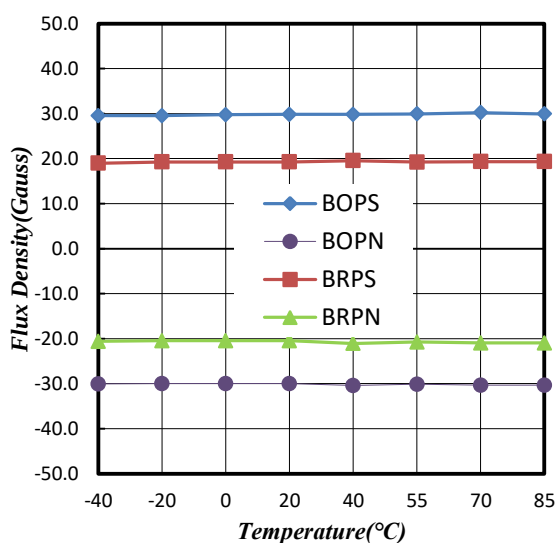


Performance Graph

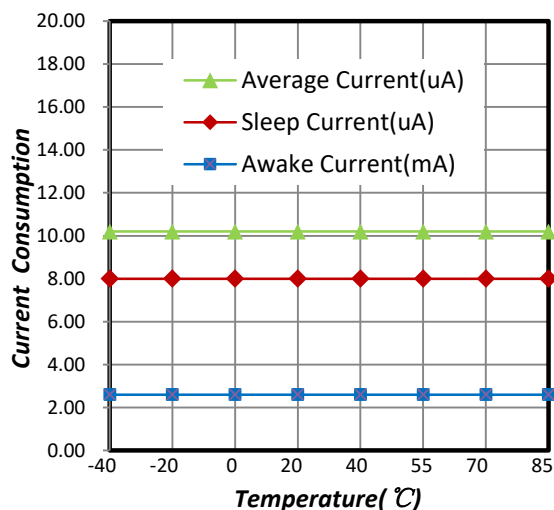
Typical Supply Voltage(VDD) Versus Flux Density



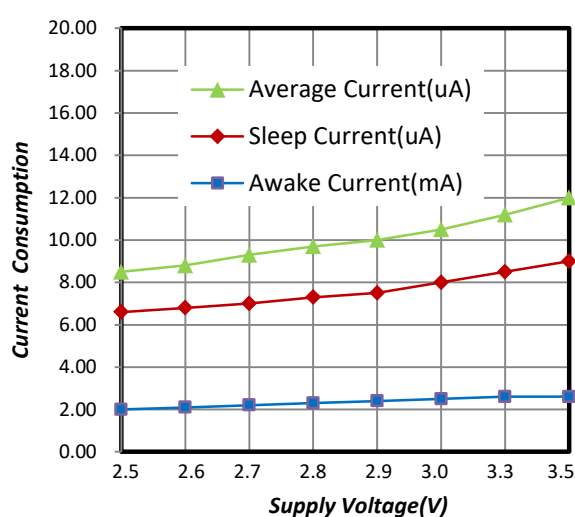
Typical Temperature(TA) Versus Flux Density



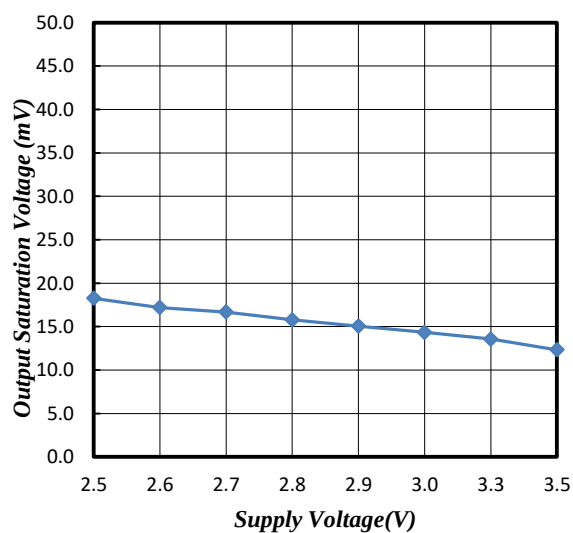
Typical Temperature(TA) Versus Supply Current(IDD)



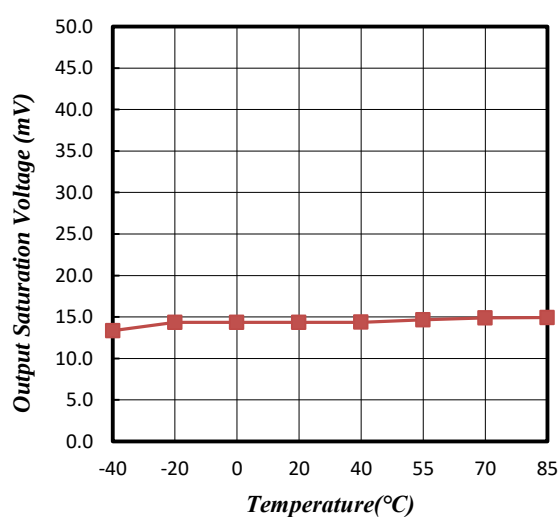
Typical Supply Voltage(VDD) Versus Supply Current(IDD)



Typical Supply Voltage(VDD) Versus Output Voltage(VDSO)

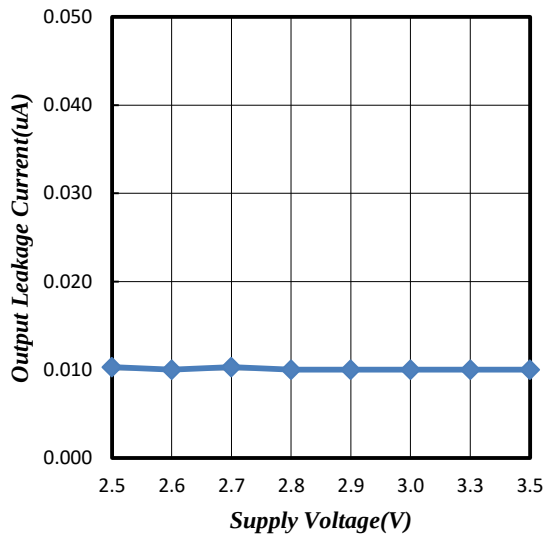


Typical Temperature(TA) Versus Output Voltage(VDSO)

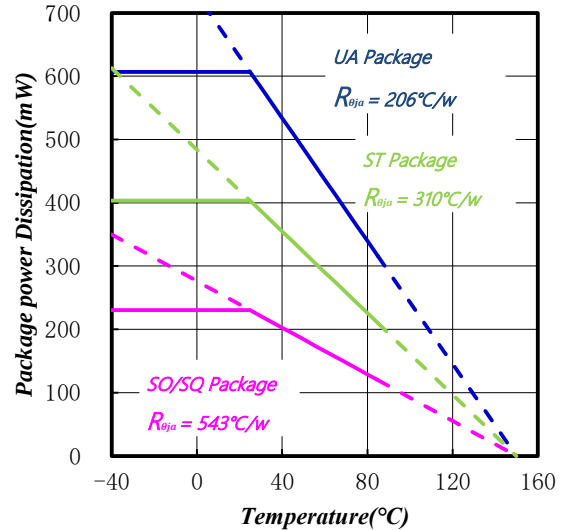




Typical Supply Voltage(VDD) Versus Leakage Current(IOFF)



Power Dissipation versus Temperature(TA)



Package Power Dissipation

The power dissipation of the Package is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_a . Using the values provided on the data sheet for the package, PD can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_a}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_a of 25 °C, one can calculate the power dissipation of the device which in this case is 230 milliwatts.

$$P_D(SO) = \frac{150^{\circ}\text{C} - 25^{\circ}\text{C}}{543^{\circ}\text{C/W}} = 230\text{mW}$$

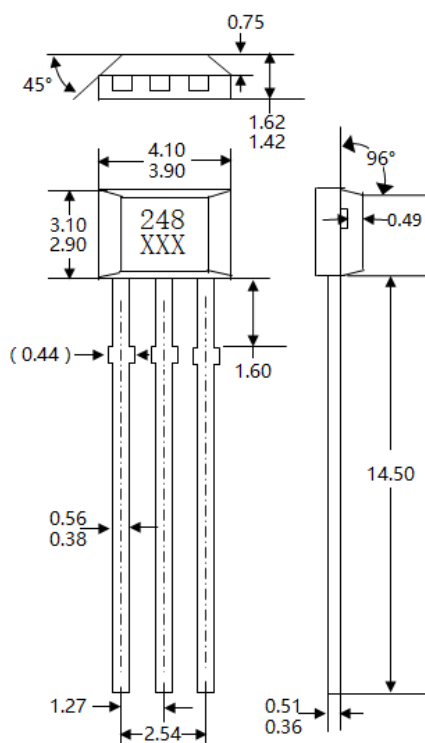
The 543°C/W for the SO package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 230 milliwatts. There are other alternatives to achieving higher power dissipation from the Package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.



Sensor Location, Package Dimension and Marking

KM1248 Package

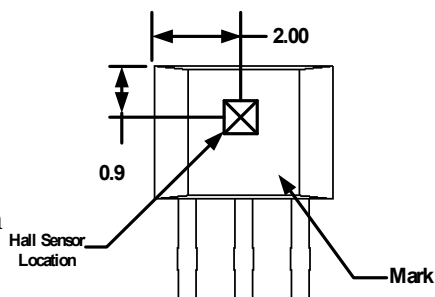
UA Package



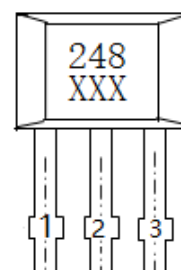
NOTES:

- 1). Controlling dimension: mm
- 2). Leads must be free of flash and plating voids
- 3). Do not bend leads within 1 mm of lead to package interface.
- 4). PINOUT:
Pin 1 V_{DD}
Pin 2 GND
Pin 3 Output

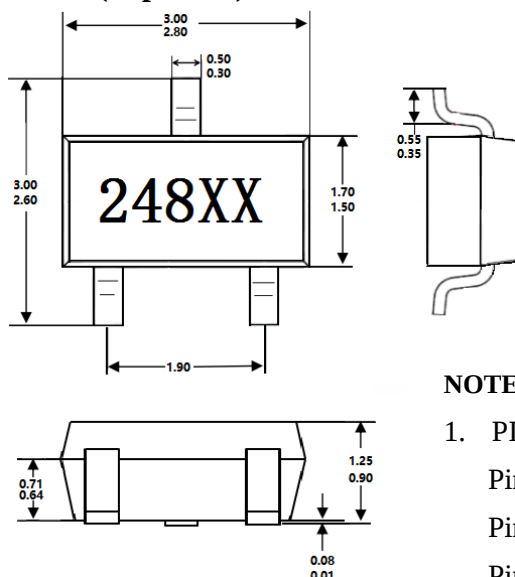
Hall Chip location



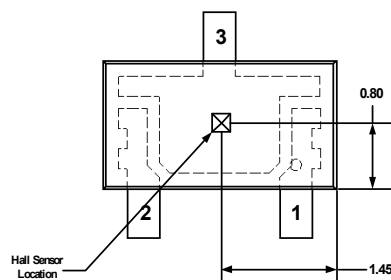
Output Pin Assignment (Top view)



SO Package (Top View)



Hall Plate Chip Location (Bottom view)

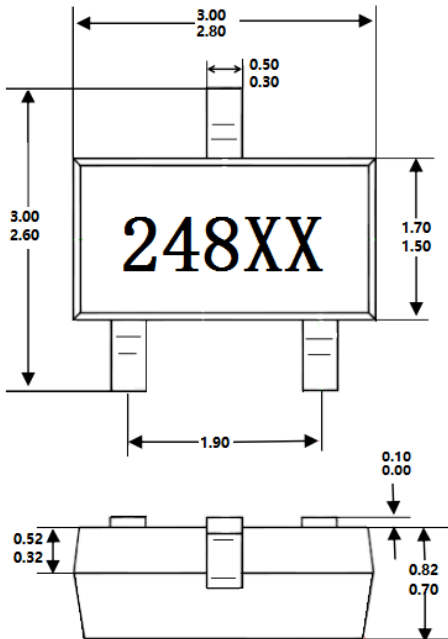


NOTES:

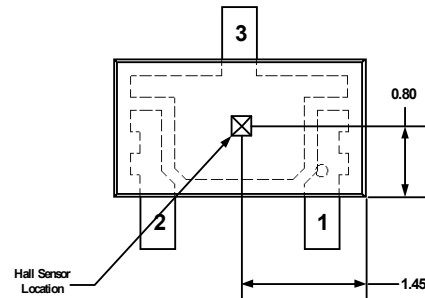
1. PINOUT (See Top View at left :)
Pin 1 V_{DD}
Pin 2 Output
Pin 3 GND
2. Controlling dimension: mm
3. Lead thickness after solder plating will be 0.254mm maximum



ST Package (Top View)



Hall Plate Chip Location (Bottom view)

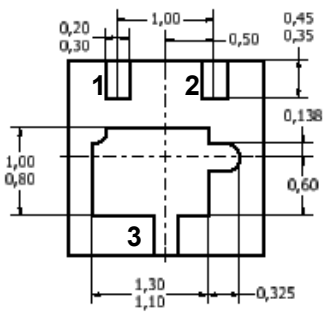
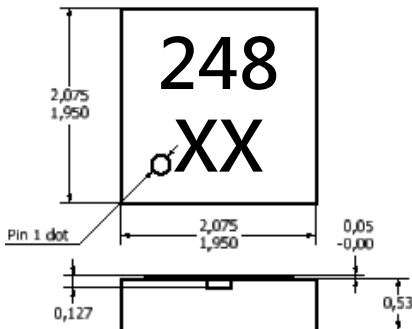


NOTES:

- PINOUT (See Top View at left):
Pin 1 VDD
Pin 2 Output
Pin 3 GND
- Controlling dimension: mm

SQ Package

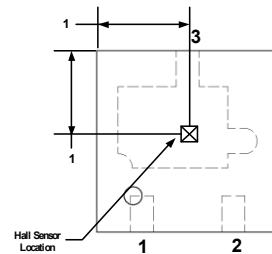
(Top View)



(Bottom View)

Hall Plate Chip Location

(Top view)

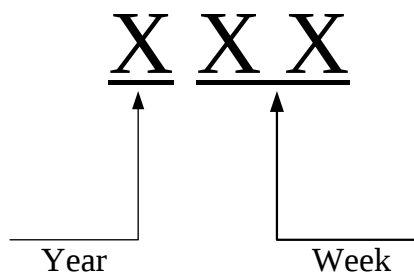


NOTES:

- PINOUT (See Top View at left):
Pin 1 VDD
Pin 2 Output
Pin 3 GND
- Controlling dimension: mm;
- Chip rubbing will be 10mil maximum;
- Chip must be in PKG. center.

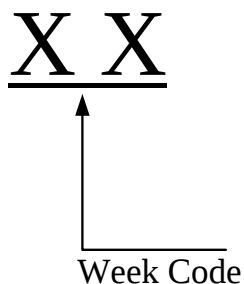


KM1248UA(TO-92S) Package Date Code



EX : 2017 Year_8 Week → 708

KM1248 SO(SOT-23)/ ST(TSOT-23)/ SQ(QFN2020-3) Package Date Code

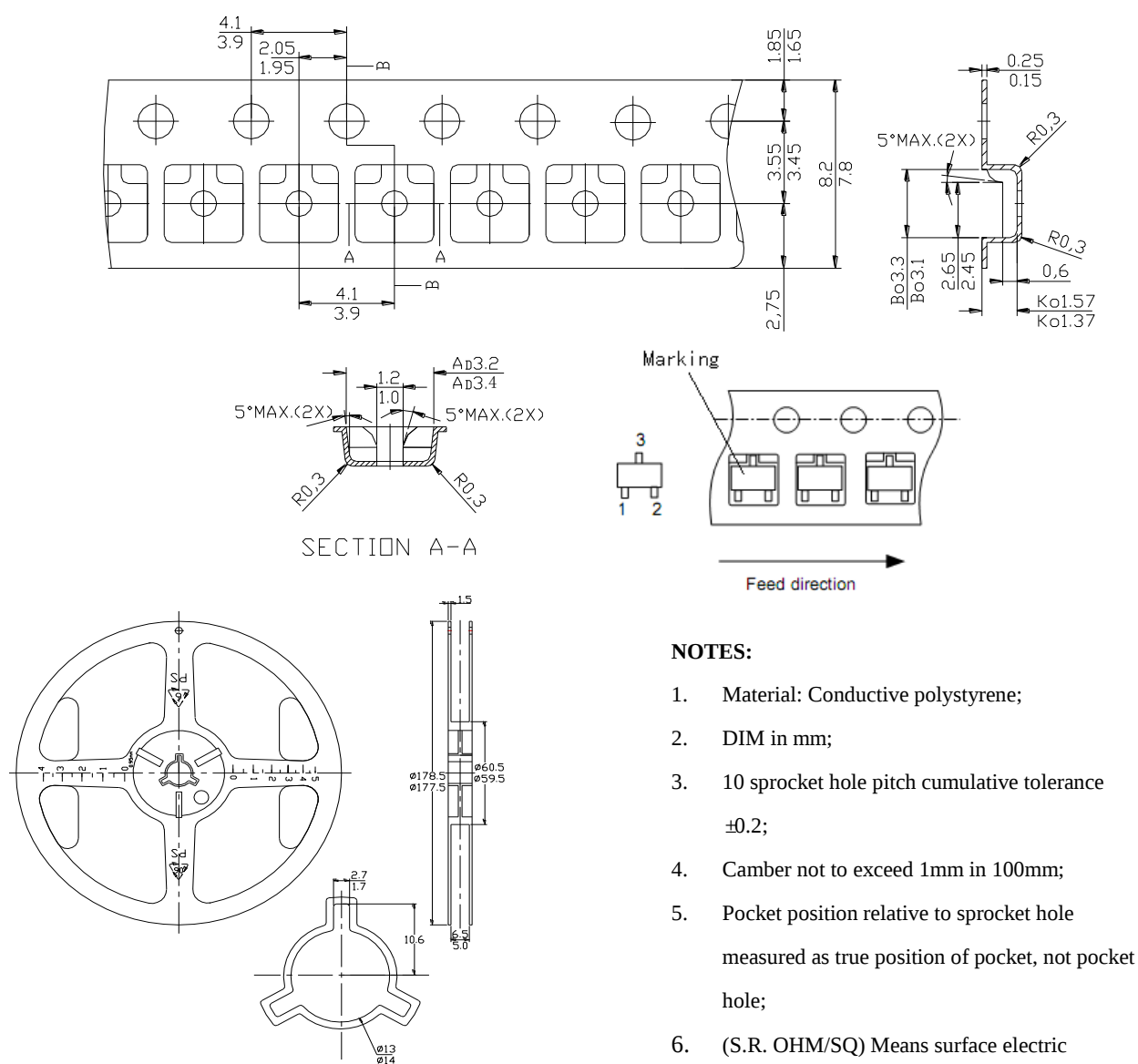


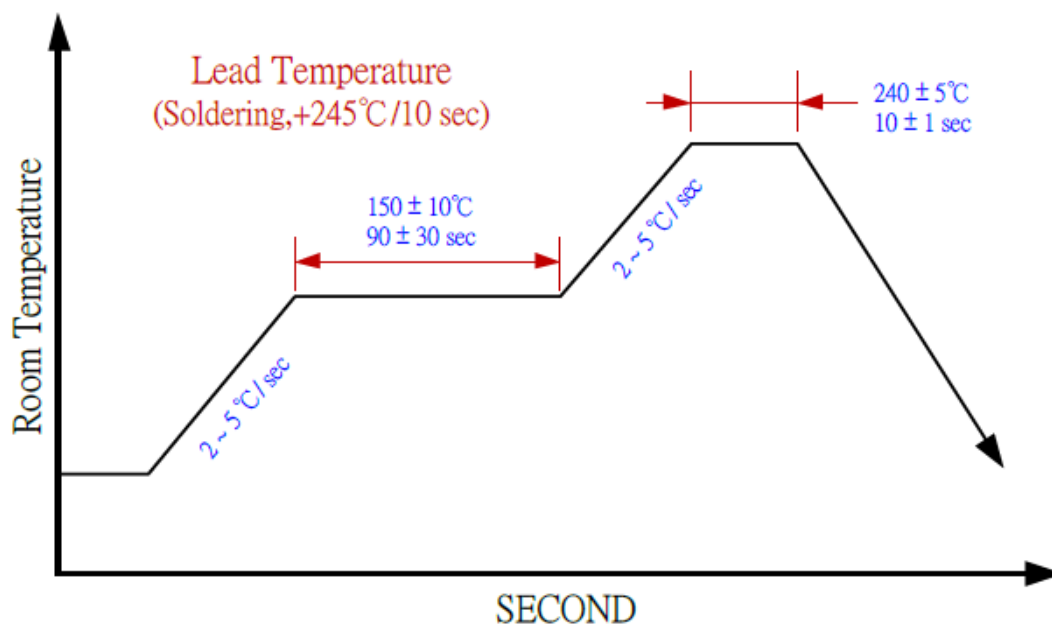
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week	14	15	16	17	18	19	20	21	22	23	24	25	26
code	YN	YO	YP	YQ	YR	YS	YT	YU	YV	YW	YX	YY	YZ
week	27	28	29	30	31	32	33	34	35	36	37	38	39
code	ZA	ZB	ZC	ZD	ZE	ZF	ZG	ZH	ZI	ZJ	ZK	ZL	ZM
week	40	41	42	43	44	45	46	47	48	49	50	51	52
code	ZN	ZO	ZP	ZQ	ZR	ZS	ZT	ZU	ZV	ZW	ZX	ZY	ZZ

EX : 2017 Year_8 Week → YH



SOT-23 & TSOT-23 package Tape On Reel Dimension





UA Soldering Condition

Packing specification:

Package	Bag	Box	Carton
TO-92S-3L	1,000pcs/bag	10bag/box	8 box/carton
SOT-23-3L	3,000pcs/reel	10 reel/box	2box/carton
TSOT-23-3L	3,000pcs/reel	10 reel/box	2box/carton
QFN2020-3	3,000pcs/reel	10 reel/box	2box/carton

TO-92S-3L	Weight	SOT-23-3L TSOT-23-3L	Weight	QFN2020-3	Weight
1000pcs/bag	0.11kg	3000pcs/reel	0.18kg	3000pcs/reel	0.13kg
10 bags/box	1.24kg	10 reels/box	1.99kg	10 reels/box	1.40kg
8 boxes/carton	10.09kg	2 boxes/carton	4.9kg	2boxes/carton	3.70kg