DH254 Hall-effect sensor is a temperature stable, stress-resistant, Low Tolerance of sensitivity micro-power switch. Superior high-temperature performance is made possible through a dynamic offset cancellation that utilizes chopper-stabilization. This method reduces the offset voltage normally caused by device over molding, temperature dependencies, and thermal stress.

DH254 is special made for low operation voltage, 1.65V, to active the chip which is includes the following on a single silicon chip: voltage regulator, Hall voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, CMOS output driver. Advanced CMOS wafer fabrication processing is used to take advantage of low-voltage requirements, component matching, very low input-offset errors, and small component geometries. This device requires the presence of unipolar magnetic fields for operation.

The package type is in a Halogen Free version has been verified by third party Lab.

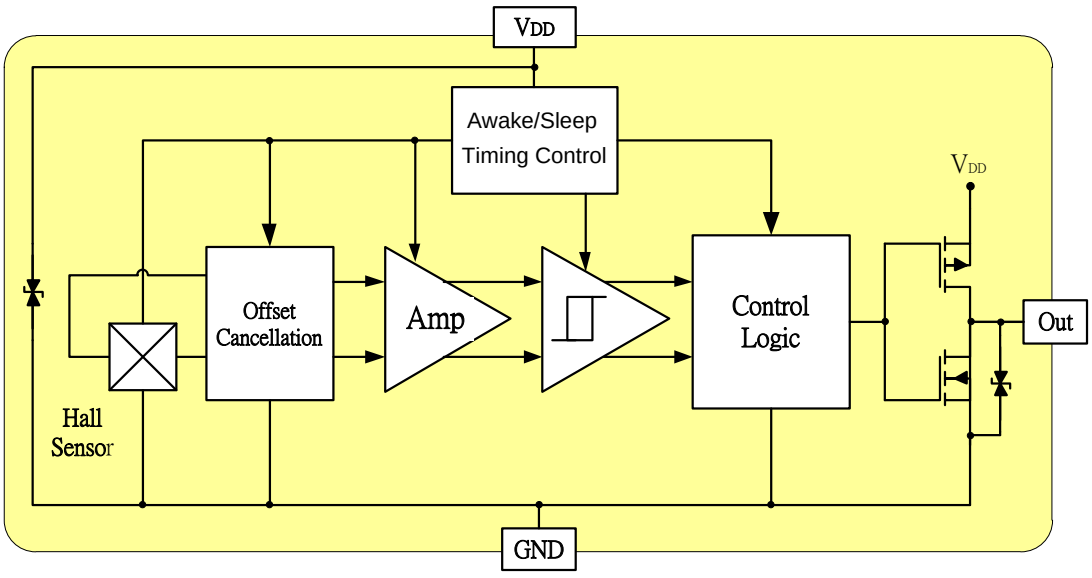
Features and Benefits

- CMOS Hall IC Technology
- Strong RF noise protection
- 1.65 to 6V for battery-powered applications
- Operation down to 1.65V, Unipolar Hall Switch Micro power consumption
- High Sensitivity for reed switch replacement applications
- Low sensitivity drift in crossing of Temp. range
- Ultra Low power consumption at 5uA (Avg)
- High ESD Protection, HBM > ±4KV(min)
- Totem-pole output
- RoHS compliant 2011/65/EU and Halogen Free

Applications

- Solid state switch
- Handheld Wireless Handset Awake Switch (Flip Cell/PHS Phone/Note Book/Flip Video Set)
- Magnet proximity sensor for reed switch replacement in low duty cycle applications
- Water Meter
- PDA
- PDVD
- NB
- Pad PC

Functional Diagram



***Note**: Static sensitive device; please observe ESD precautions. Reverse V_{DD} protection is not included. For reverse voltage protection, a 100Ω resistor in series with V_{DD} is recommended.*

DH254, HBM > ±4KV which is verified by third party lab.

Absolute Maximum Ratings *At(Ta=25℃)*

Characteristics		Values	Unit
Supply voltage, (V_{DD})		7	V
Output Voltage, (V_{out})		7	V
Reverse Voltage, (V_{DD}) (V_{OUT})		-0.3	V
Magnetic flux density		Unlimited	Gauss
Output current, (I_{OUT})		1	mA
Operating temperature range, (Ta)		-40 to +85	℃
Storage temperature range, (Ts)		-65 to +150	℃
Maximum Junction Temp, (Tj)		150	℃
Thermal Resistance	(θ_{JA}) ST/SN/UA/SQ/SS	310/540/206/540/540	℃/W
	(θ_{JC}) ST/SN/UA/SQ/SS	223/390/148/390/390	℃/W
Package Power Dissipation, (P_D) ST/SN/UA/SQ/SS		400/230 /606/230/230	mW

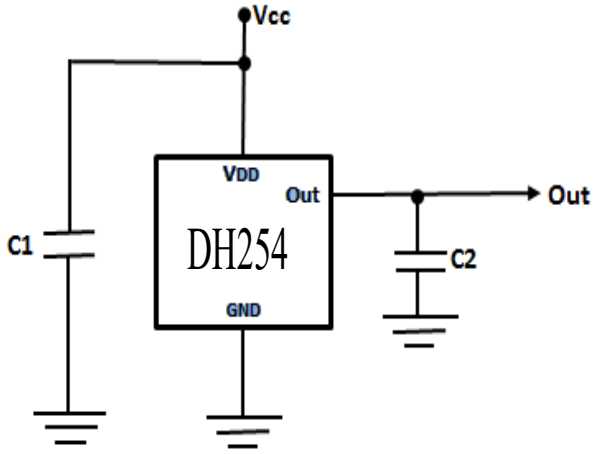
Note: *Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.*

Electrical Specifications

DC Operating Parameters ：Ta=25℃, V_{DD}=1.8V

Parameters	Test Conditions	Min	Typ	Max	Units
Supply Voltage, (V_{DD})	Operating	1.65		6	Volts
Supply Current, (I_{DD})	Awake State		1.4	3	mA
	Sleep State		3.6	7	μA
	Average		5	10	μA
Output Leakage	Output off			1	uA
Output High Voltage, (V_{OH})	I_{OUT}=0.5mA(Source)	V_{DD}-0.2			V
Output Low Voltage, (V_{OL})	I_{OUT}=0.5mA(Sink)			0.2	V
Awake mode time, (Taw)	Operating		40	80	uS
Sleep mode time, (T_{SL})	Operating		40	80	mS
Duty Cycle, (D,C)			0.1		%
Electro-Static Discharge	HBM	4			KV

Typical application circuit



C1：10nF

C2：100pF

Magnetic Specifications

DC Operating Parameters ：Ta=25℃, V_{DD}=2.0V

Parameter	*Symbol*	*Test Conditions*	*Min.*	*Typ.*	*Max.*	*Units*
Operating Point	B_{OP}	N pole to branded side, B > BOP, Vout On	-50	-30		Gauss
Release Point	B_{RP}	N pole to branded side, B < BRP, Vout Off		-20	-10	Gauss
Hysteresis	B_{HY}	|BOPx - BRPx|		10		Gauss

Magnetic Specifications

DC Operating Parameters ：Ta=25℃, V_{DD}=2.0V

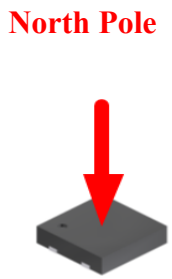
Parameter	*Symbol*	*Test Conditions*	*Min.*	*Typ.*	*Max.*	*Units*
Operating Point	B_{OP}	S pole to branded side, B > BOP, Vout On		30	50	Gauss
Release Point	B_{RP}	S pole to branded side, B < BRP, Vout Off	10	20		Gauss
Hysteresis	B_{HY}	|BOPx - BRPx|		10		Gauss

DH354ES T/SQ/SS/SN/UA Output Behavior versus Magnetic Polar

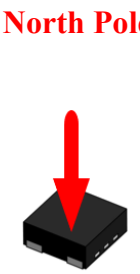
DC Operating Parameters：Ta = -40 to 85℃, V_{DD} =1.65V to 6V

Parameter	*Test condition*	*OUT（ST/SS/SQ/UA）*	*Parameter*	*Test condition*	*OUT(SN）*
Null or weak magnetic field	B=0 or B < BRP	High	**Null or weak magnetic field**	B=0 or B < BRP	High
North pole	B<Bop-N	Low	**South pole**	B>Bop-S	Low

ST Package

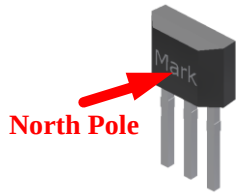


SQ Package

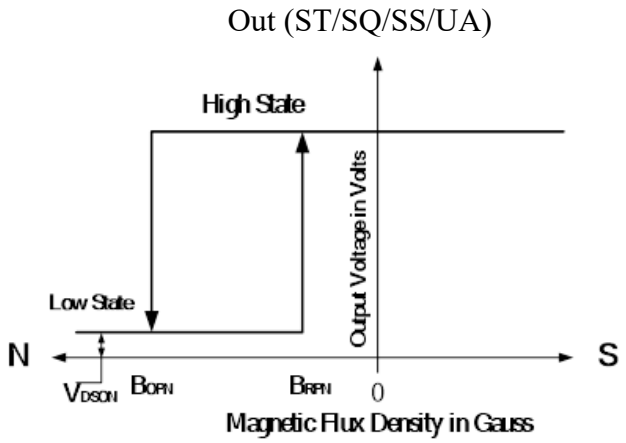


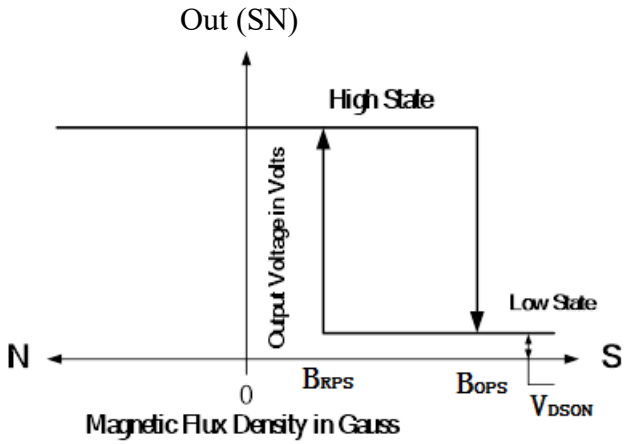
SS Package

SN Package



UA Package





Package Power Dissipation

The power dissipation of the Package is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, Ta. Using the values provided on the data sheet for the package, PD can be calculated as follows:

$$P_D = \frac{T_{J(max)} - Ta}{R_{\theta ja}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature Ta of 25°C, one can calculate the power dissipation of the device which in this case is 400 milliwatts.

$$P_D(ST) = \frac{150℃ - 25℃}{310℃/_W} = 400mW$$

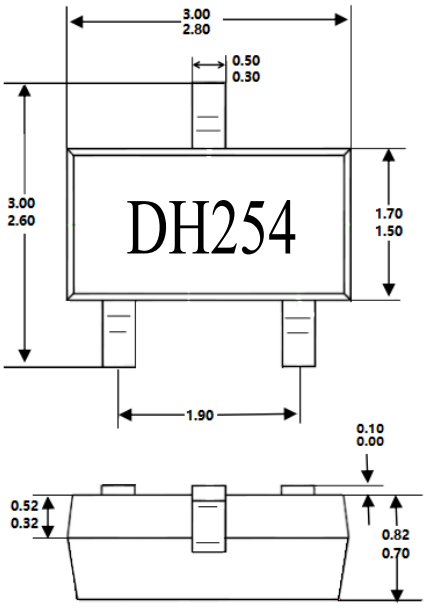
The 310℃/W for the SN package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 400 milliwatts. There are other alternatives to achieving higher power dissipation from the Package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

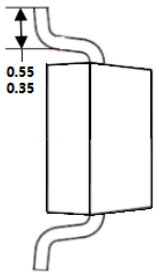
Sensor Location, package dimension and marking

MH254 Package

ST Package(TSOT-23)

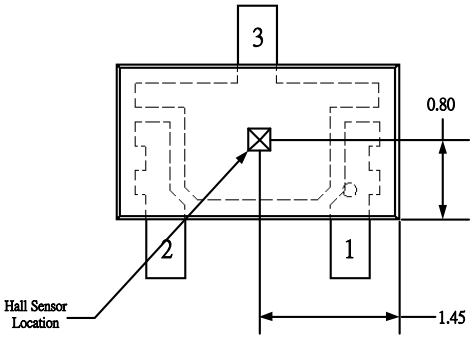
(Top View)





Hall Plate Chip Location

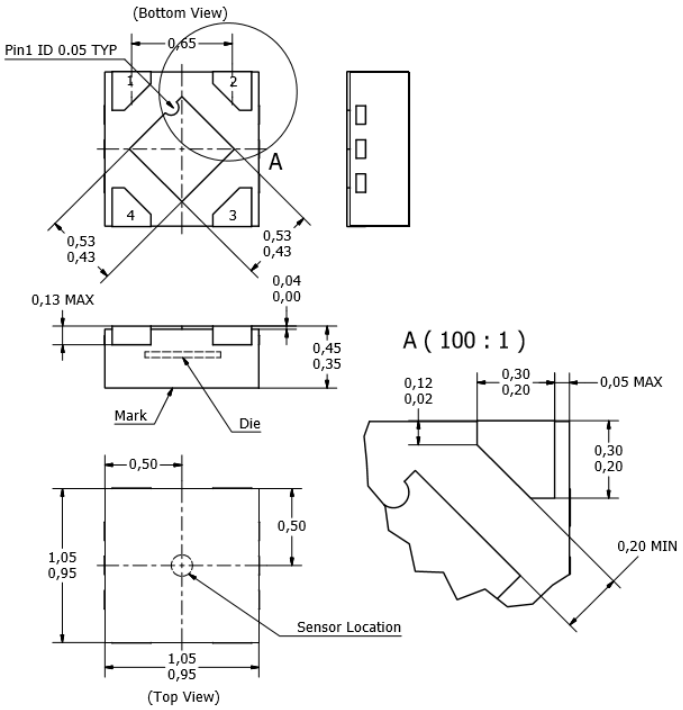
(Bottom view)



NOTES:

1. PINOUT (See Top View at left:)
   Pin 1 VDD
   Pin 2 Output
   Pin 3 GND
2. Controlling dimension: mm;

SS Package (DFN 1.0*1.0)

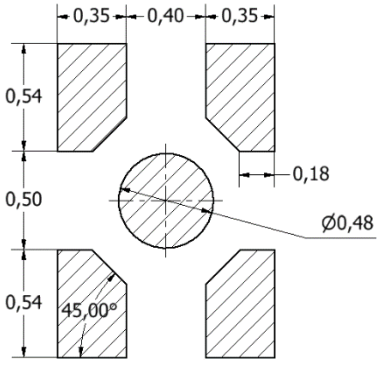


NOTES:

1. Controlling dimension: mm
2. Leads must be free of flash and plating voids
3. Lead thickness after solder plating will be 0.254mm maximum
4. PINOUT:

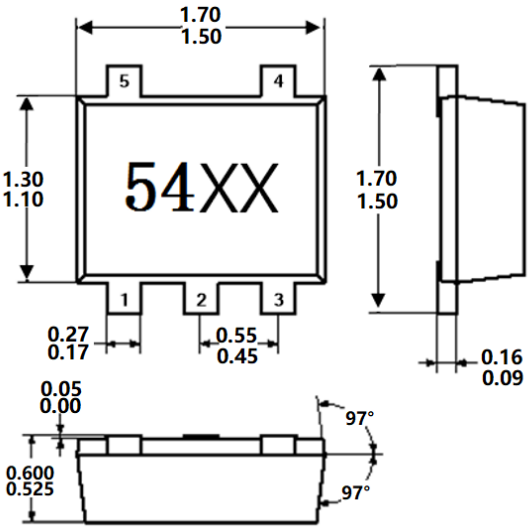
Pin No.	Pin Name	Function
1	V_{DD}	Power Supply
2	GND	Ground
3	SPD	
4	V_{OUT}	Output

5. (For reference only)Land Pattern



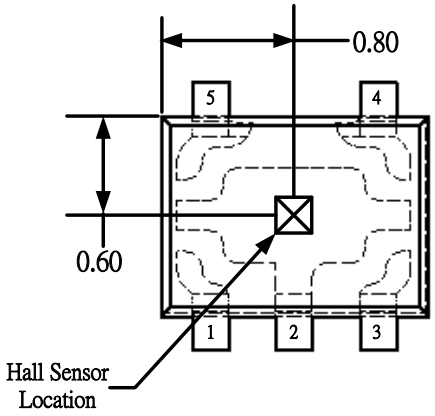
SN Package (SOT-553)

(Top View)



Hall Plate Chip Location

(Top View)

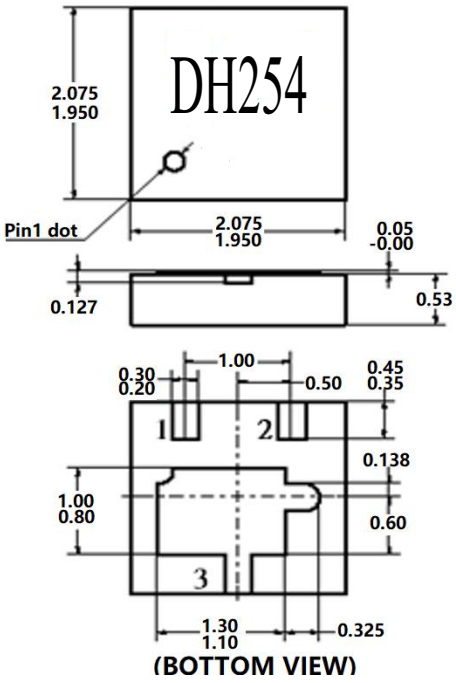


NOTES:

1. PINOUT (See Top View at left:)
   - Pin 1 NC
   - Pin 2 GND
   - Pin 3 NC
   - Pin 4 VDD
   - Pin 5 Out
2. Controlling dimension: mm;

SQ Package (QFN2020-3)

(Top View)



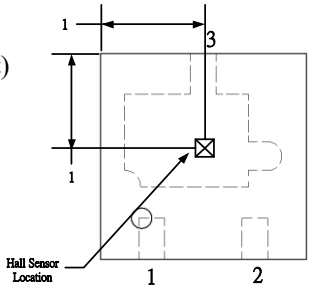
(BOTTOM VIEW)

NOTES:

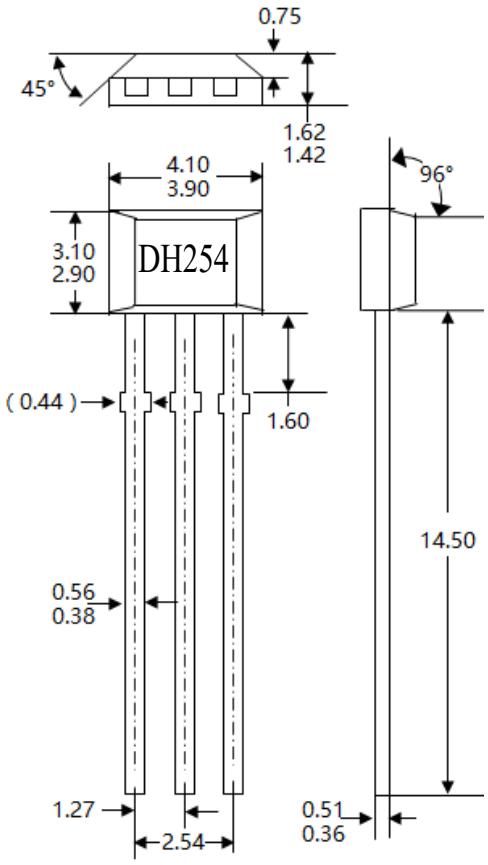
3. PINOUT (See Top View at left)
   Pin 1 VDD
   Pin 2 Output
   Pin 3 GND
4. Controlling dimension: mm;
5. Chip rubbing will be 10mil maximum;
6. Chip must be in PKG. center.

Hall Plate Chip Location

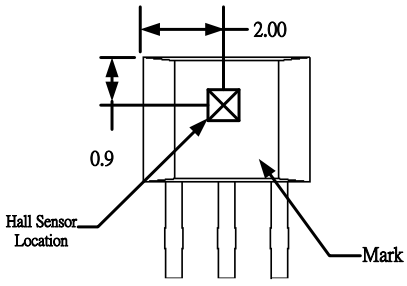
(Top view)



UA Package (TO-92S)

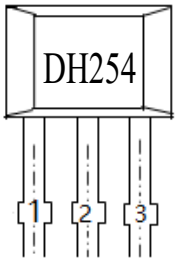


Hall Chip location



Output Pin Assignment

(Top view)



NOTES:

1).Controlling dimension: mm

2).Leads must be free of flash and plating voids

3).Do not bend leads within 1 mm of lead to package interface.

4).PINOUT:

Pin 1 VDD

Pin 2 GND

Pin 3 Output